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# Modeling the cutoff frequency of single-heterojunction bipolar transistors subjected to high collector-layer current

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High current densities in the collector layer reduce the cutoff frequency of heterojunction bipolar transistors. We develop a model based on analytical expressions that describe this reduction. These expressions represent the contributions from each of six regions defined in the output current-voltage characteristic. The model has parameters determined entirely by device physical makeup. It has no fitting parameters. Its predictions agree well with experimental data taken on two $N/p^+/n$ aluminum-gallium-arsenide/gallium-arsenide transistors having abrupt junctions grown by molecular-beam epitaxy. Because previous models omitted the effects of high current densities, their predictions agree less favorably. The development of the model considers the effects that compound-semiconductor properties such as velocity overshoot have on the cutoff frequency.

## I. INTRODUCTION

Compound-semiconductor $N/p^+/n$ heterojunction bipolar transistors (HBTs) provide high electron mobility in the base layer. Also they allow the flexibility to choose low emitter and high base doping concentrations. These properties make possible high nonlinearity (high transconductance), high cutoff frequency $f_T$, and excellent threshold voltage uniformity and insensitivity to fabrication processing variations. Thus the heterojunction bipolar transistor has become considered an attractive technology choice for ultrahigh-speed logic and other applications.[1,2] (The notation $N/p^+/n$ means an $n$-type *wide-gap* emitter layer bordering a heavily doped $p$-type base layer in a single-heterojunction bipolar transistor structure.)

Large transconductance and excellent threshold voltage uniformity are properties also shared by the silicon homojunction technology. The possible advantage of the compound-semiconductor heterojunction bipolar technology is its potential for higher speed and cutoff frequency. Physical mechanisms that lower the cutoff frequency compromise this potential. Such mechanisms exist in any bipolar technology designed for high switching speeds because speed with reasonable fanout requires quick charging of all capacitances, including parasitic and interconnect capacitances. To charge these capacitances quickly, high current densities must flow through collector layers.

High collector-layer currents lower the cutoff frequency or speed by a system of mechanisms that have various names: Kirk effect, base pushout, current-induced base widening, and quasisaturation. Tang, MacWilliams, and Solomon demonstrated these high-current effects experimentally, and systematically analyzed and emphasized their importance for the circuit design of silicon digital integrated circuits.[3,4] In the device-physics literature of heterojunction bipolar transistors, however, no analytical treatment of these effects as yet exists.

Among the papers written on HBT cutoff frequency performance, most[5-7] stressed HBT fabrication and experimental evidence of high cutoff frequency and speed. For example, an experimental $f_T = 105$ GHz and an experimental unity fanout emitter-coupled-logic gate delay of 1.9 ps have been reported.[8] Other papers[9-11] reported numerical results about the cutoff frequency characteristics. Shur[12] presented an analytical treatment of the cutoff frequency, but he omitted the consequences that high collector currents in a collector layer have on $f_T$. In this paper, we describe these consequences by analytical expressions.

In Sec. II, we sketch the physical mechanisms that cause high collector-layer current to lower the cutoff frequency. In Sec. III, using gallium arsenide as an example, we focus on those properties of compound semiconductors that need special attention when analyzing the cutoff frequency. The physical descriptions of Secs. II and III illustrate the system of competing physical mechanisms associated with high collector current in a moderately or lightly doped collector layer. It emphasizes that different mechanisms predominate in different regions of the collector current versus collector voltage characteristic. Separating this characteristic into different regions will be a key to the analysis presented in Sec. IV. That analysis yields a model for the cutoff frequency that has parameters determined entirely by device physical makeup, with no fitting parameters employed. The model developed in Sec. IV applies to a heterojunction bipolar transistor that has an emitter-base heterojunction but a base-collector homojunction. In this paper it is outside our reach to include double-heterojunction bipolar transistors. In Sec. V, we show that the predictions of our model agree well with experimental data taken on two $N/p^+/n$ aluminum-gallium-arsenide/gallium-arsenide heterojunction bipolar transistors having abrupt junctions grown by molecular-beam epitaxy.

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## II. PHYSICAL MECHANISMS

The physical mechanisms occurring in the collector layer that decrease the cutoff frequency have been described by both university and industrial researchers.[13-18] The mechanism that dominates depends on the transistor makeup and on the circuit environment in which the transistor resides.[14] To sketch the physics of these mechanisms, without loss in generality, we may consider an $n/p/n$ transistor and picture the events that happen as the collector current is increased.

The $n$-type collector layer has a donor atom concentration chosen in the design so that the transistor can withstand a particular magnitude of collector voltage while avoiding avalanche breakdown. At a given temperature, this dopant concentration determines the resistance of the collector layer. An increase of the current flowing through the collector resistance increases the voltage across the internal collector/base junction in a forward direction. For a given collector resistivity, if the externally applied collector voltage is sufficiently low,[14] increases in collector current will eventually cause the internal collector-base junction to become forward biased. In this range of low collector currents, the collector current-voltage characteristics and the frequency response of the current gain can be modeled simply by accounting for the voltage drop across a nearly constant intrinsic resistor.

As current increases further, however, the rising forward voltage injects more electrons and holes into the collector/base space-charge layer. Eventually, the consequent screening obliterates the collector/base barrier that at lower current had straddled the collector metallurgical junction.[19] Then a high-injection, electron-hole plasma extends partly into the collector layer. On its edge nearest the collector contact, this thickened quasineutral layer is bordered by a thin electron accumulation layer, formed because the positive potential applied to the collector contact and the resulting electric field decreases the hole density in this accumulation layer. Farther toward the collector contact, a third layer forms. In this layer, the current is carried by the drift of an equilibrium density of electrons in a large electric field.

As the current and thus the electric field in this third layer increases further, the electron drift velocity becomes less dependent on the electric field. For large enough electric field, we will assume for now that the electron drift velocity saturates or becomes independent of the electric field. This saturation occurs in silicon. In Sec. III we will explore the conditions for which such saturation will serve as a good approximation in gallium arsenide transistors. Given the assumptions of a saturated electron drift velocity and an increasing collector current, the current will eventually reach a critical level. That critical level will be reached when the equilibrium density of electrons determined by the dopant concentration in the collector layer can no longer support the current. Thus electrons must accumulate in this third layer as increased current is forced through it. This space-charge layer of electrons attracts within it holes from the base layer ohmic contact. Thus the resulting quasineutral hole-electron plasma expands further into the collector layer, pushing ahead of it the space-charge layer of accumulated electrons. This sequence of events makes the effective base thickness progressively greater as the current increases. Thus the current gain and frequency response continue to decline faster with increasing collector current than they would if the base thickness had remained constant.

In contrast to the preceding description, in which the applied collector voltage was assumed to be relatively small, assume now that the reverse voltage applied to the collector is larger than some critical value.[14] Then the voltage drop across the internal collector resistance becomes a secondary mechanism and the sequence of events described up to now is replaced by a different sequence. As a primary mechanism in this sequence, which prevails over a range of collector current, the electron-charge density constituting the collector current cancels part of the positive dopant ion-charge density in the collector layer. Thus a thicker space-charge layer is required to sustain the voltage difference between the collector and base. As the collector current increases, this space-charge layer expands further into the collector layer. (In contrast, in the previously described sequence, the space-charge layer contracted rather than expanded with increasing collector current.) Beyond a certain level of collector current, the electrons contributed by this current outnumber the donor ions. The space charge of the layer, dominated by electrons, becomes negatively rather than positively charged. At higher ranges of collector current, the limited drift velocity attainable by the electrons provokes more electrons to accumulate and holes are attracted in from the base contact. The resulting hole-electron quasineutral plasma thus expands with increasing current. This thickens the effective base layer, and reduces the current gain and $f_T$ of the transistor.

## III. VELOCITY OVERSHOOT AND ALLIED PHENOMENA

The energy-momentum characteristics in silicon and gallium arsenide differ. Silicon is an indirect-gap semiconductor in which the direct-gap minimum is several electron volts higher than the indirect-gap minimum for the conduction band. Thus, in silicon, the rate of electron transitions between the indirect-gap valley and the direct-gap valley is very low. In contrast, in gallium arsenide an indirect-gap valley or upper valley ($L$ valley along the $\langle 111 \rangle$ direction) is only about 0.35 eV above the direct-gap or $\Gamma$ valley. In a given layer in a gallium arsenide device, these intravalley electron transitions occur at a rate determined by three factors.

(1) If the electrons enter the layer with low kinetic energy, the total voltage across the layer under study must exceed 0.35 V. The more it exceeds 0.35 eV, the higher the rate of transitions will be. In practical circuits, the depletion layer of the collector-base junction is the layer having the highest voltage across it. Thus the voltage applied across the collector-base terminals determines, in part, the rate of transitions between the $\Gamma$ and $L$ valleys.

(2) The longer the free path is, the greater the transition rate will be. Because phonon collisions determine the free path, lowering the temperature will increase the transition rate.

(3) The higher the kinetic energy of the electrons incident on the layer is, the greater the transition rate will be.

The transitions start from the narrow (low effective mass) conduction-band minimum at the $\Gamma$ valley (corresponding to wave vector $k=0$). They end in the many siliconlike $L$ valleys. These transitions significantly reduce electron mobility and electron saturation drift velocity. This occurs not only because of the larger effective mass in the $L$ valleys but also because of the strong intervalley scattering. The experimental steady-state characteristics of drift velocity versus electric field demonstrate these reductions.[2] For gallium arsenide, a drift velocity peak of $2.2\times10^7$ cm/s occurs at an electric field of about 3 kV/cm. For higher values of electric field, the velocity first falls and then, for electric fields above about 14 kV/cm, saturates at a value of $1.5\times10^7$ cm/s.

As noted in Sec. II, the drift velocity characteristics at high electric fields enter prominently into the high-current effects that lower the cutoff frequency. As implied by Eden,[2] however, the empirical steady-state characteristic just described applies only to heterojunction bipolar transistors used in power applications.[20] In such applications, the large voltage between the collector and base terminals resembles experimental conditions that were used to determine the GaAs experimental velocity against field characteristic. In low-voltage digital applications, such as emitter-coupled logic (ECL), the maximum voltage between the collector and base terminals is one diode drop. For gallium arsenide, this is about 1 V. For such circuits, the rate of electron transitions between the lower and upper valleys is small. Not only does the small voltage limit the transition rate. It is also limited by the short electron transit time across the collector depletion layer. This transit time of about 1 ps is so short that transitions are unlikely to occur.

If conditions prevent electron transfer from the $\Gamma$ valley, the steady-state drift velocity in the collector depletion layer can exceed the saturation value of $10^7$ cm/s by nearly an order of magnitude. The physics underlying this occurrence is straightforward. Near the edge of the collector-base depletion layer, the electric field changes abruptly. Subjected to this steeply rising magnitude of electric field, some electrons in the distribution gain considerable kinetic energy before collisions can occur to transfer that energy to the lattice. Thus the velocity averaged over the ensemble of electrons exceeds the saturation velocity, which experimentally was determined by subjecting a semiconductor to a spatially constant electric field.

The key point is that the conventional theory for the electron drift velocity relies on the assumption that the drift velocity is a function of the local electric field. But large gradients of the local electric field (corresponding to nearly jump discontinuities in the band edge) can also influence the velocity. Thus not only does the local electric field (or, more precisely, the local quasifield) at a macroscopic point influence the drift velocity; it also depends on the electric field nearby and thus on derivatives of the electric field. As noted, in heterojunction bipolar transistors, large gradients of the electric field can exist near the base edge of a reverse-biased base-collector depletion layer. As device dimensions shrink and such gradients of the electric field increase, the drift velocities in this depletion layer may exceed those predicted by conventional drift-diffusion theory. It is said that velocity overshoot occurs.

The quantitative treatment of these velocity overshoot or ballistic effects is complicated. Such treatments must include the details of the energy-momentum relation both in the $\Gamma$ and $L$ valleys and details of the phonon and defect distributions. Despite these complications, it is clear that these velocity overshoot or ballistic effects could increase the cutoff frequency by reducing the transit time across the collector-base depletion layer.

To assess how large is the increase in cutoff frequency, we refer to the results of theoretical Monte Carlo evaluations of electron transport in heterojunction bipolar transistors. Monte Carlo (particle) methods and energy-transport models based on higher moments of the Boltzmann equation applied to heterojunction bipolar transistors show that the electron drift velocity in the collector layer exceeds the drift saturation velocity $v_s$ [$v_s\approx1.5\times10^7$ cm/s for GaAs at $T=300$ K (Ref. 2)]. But such studies show for the device structures examined that this velocity overshoot negligibly influences the total transit time. Thus it negligibly influences the cutoff frequency.[10,11,21]

Accordingly, in our analysis, we shall set the electron drift velocity equal to the saturation velocity. Reviewing the three factors listed at the beginning of Sec. III, we see that this approximation will introduce least error if the following conditions hold: (1) The transistors are used in digital circuits such as ECL gates in which the applied voltage across the collector-base junction is low; (2) the base-layer chemical and doping compositions are spatially constant so that the quasifield acting on electrons is low in the base and the electrons enter the collector depletion layer with low kinetic energy. For power applications, in which large voltages appear across the collector-base terminals, the approximation is questionable. Then the steady-state characteristic of electron velocity versus electric field would apply.

The approximation is also questionable if the aluminum mole fraction is varied spatially to yield a graded-base HBT in which the energy gap varies with position. Then the kinetic energy distribution of electrons existing the base layer and entering the collector depletion layer could cause velocity overshoot to contribute to increasing the cutoff frequency.

## IV. THEORY

We begin with the conventional theory of the cutoff frequency to point out dissimilarities between homojunction theory and theory for heterojunction bipolar transistors.

Consider an $N/p^+/n/n^+$ single-heterojunction bipolar transistor with abrupt doping profiles (Fig. 1). The cutoff frequency $f_T$ of the HBT can be expressed as[12]

$$f_T\approx1/[2\pi(\tau_E+\tau_C+\tau_{CT}+\tau_{BT})], \tag{1}$$

where[6]

$$\tau_E=r_e(C_{TE}+C_{DE})\approx(4V_T/J_eA)(C_{TE}+C_{DE}) \tag{2}$$

is the emitter capacitance charging time, $V_T$ is the thermal voltage, $J_C$ (A/cm$^2$) is the collector-current density, $r_e$ is emitter-base junction resistance, $A$ is the junction cross-section area, $C_{DE}$ (F/cm$^2$) is the emitter-base diffusion capaci-

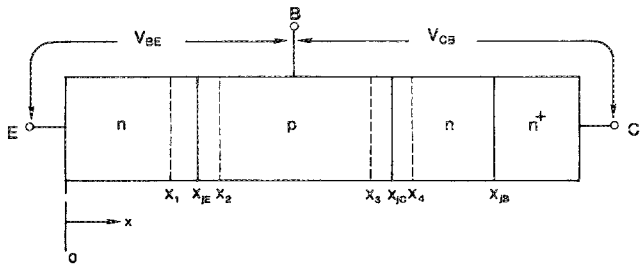


FIG. 1. Schematic illustration of a one-dimensional $n/p/n/n^+$ heterojunction bipolar transistor, indicating the emitter-base space-charge-layer edges, $X_1$ and $X_2$, and base-collector space-charge-layer edges, $X_3$ and $X_4$. It is assumed that the $n^+$ region has no effects on the collector performance.

tance, and $C_{TE}$ (F/cm$^2$) is the emitter-base heterojunction capacitance.

Although (1) and (2) appear in the homojunction transistor literature, when they are applied to the HBT certain inequalities deserve notice. First, for HBTs, over nearly the entire practical range of emitter-base applied forward voltage, the minority-carrier storage in the quasineutral emitter and base layers, characterized by $C_{DE}$, is negligible compared with the mobile electron and hole storage in the emitter-base space-charge layer, characterized by $C_{TE}$. The relative unimportance of $C_{DE}$ results because the high base doping concentration hinders the accumulation of large electron concentrations in the $p$-type base and because the large hole barrier height hinders hole injection into the $p$-type emitter layer.[1,22] Consequently, for heterojunction bipolar transistors, (2) reduces to

$$\tau_E \approx (4V_T/J_C A)C_{TE} \tag{3}$$

and $C_{TE}$ can be approximated as the conventional depletion capacitance model[23,24]:

$$C_{TE} \approx \{qN_{DE}N_{AB}\epsilon_E\epsilon_B/[2(\epsilon_E N_{DE} + \epsilon_B N_{AB}) \times (V_{biBE} - V_{BE})]\}^{0.5}. \tag{4}$$

In (4), $E$ and $B$ represent emitter and base, respectively, $\epsilon$ is the dielectric permittivity, $N_A$ is the acceptor doping concentration, $N_D$ is the donor doping concentration, and $V_{BE}$ is the emitter-base applied voltage. In contrast to homojunction transistor theory, the expression for $V_{biBE}$, the emitter-base junction built-in potential, must account for both dissimilar barrier heights and for dissimilar dielectric permittivities. That expression is[22]

$$V_{biBE} = -|\chi_B - \chi_E| - (0.5/q)|E_{GE} - E_{GB}| + V_T \ln(N_{DE}N_{AB}/n_{iE}n_{iB}) + 0.5V_T \ln(N_{CB}N_{VE}/N_{CE}N_{VB}), \tag{5}$$

where $\chi$ is the electron affinity, $n_i$ is the intrinsic concentration, $E_G$ is the energy gap, and $N_C$ and $N_V$ are the effective densities of states for the conduction and valence bands. Equation (4) neglects the influence of screening by mobile electrons and holes in the heterojunction emitter-base space-charge layer. A model developed in Refs. 25 and 26 takes this screening into account. This model provides better accuracy than (4), but is more complex.

The charging time constant for the collector capacitance is given by

$$\tau_C = r_{rc}C_{CT}A, \tag{6}$$

where $r_{rc}$ is the collector resistance and $C_{CT}$ (F/cm$^2$) is the base-collector homojunction depletion capacitance, which is given by

$$C_{CT} \approx \{qN_{AB}N_{DC}\epsilon_B/[2(N_{AB} + N_{DC})(V_{biCB} - V_{CB})]\}^{0.5}. \tag{7}$$

In (7), subscripts $B$ and $C$ represent the base and collector, $V_{CB}$ is the base-collector applied voltage ($V_{CB} > 0$ means reverse bias), and $V_{biBC}$ is the base-collector built-in junction potential.[23] Note that $\epsilon_B = \epsilon_C$ for this homojunction. The resistance $r_{rc}$ in (6) is given by

$$r_{rc} \approx \rho \times (\text{collector thickness})/(\text{base-collector area}), \tag{8}$$

where $\rho$ is the collector resistivity, which depends on the collector doping concentration. As will be shown in Sec. IV A, the collector thickness depends on the collector current.

The effective base transit time is given by the ratio of the quasineutral base thickness to the electron velocity in the base:

$$\tau_{BT} = W_B/v_{nB}. \tag{9}$$

The quasineutral base thickness ($W_B = X_3 - X_2$) (Fig. 1) depends on collector current in a manner explained in Sec. IV A. In (9), $v_{nB}$ is the minority-carrier electron velocity in the base. Based on the conventional drift-diffusion theory and an assumed negligible built-in electric field in the base layer, the expression for the mean electron diffusion velocity is

$$v_{nB} \approx 2D_{nB}/W_B, \tag{10}$$

where $D_{nB}$ is the electron diffusion coefficient. The assumption that no built-in electric field in the base layer requires that there are no gradients of the doping density or of the energy gap. If such an electric field exists, an analytical expression for the mean electron velocity can still be derived for the special case that the electric field is independent of position. In this paper, however, we focus on a single-heterojunction bipolar transistor, which implies a homojunction collector-base capacitance. Thus we limit attention to (10).

The validity of (10) is also open to question because for devices having small dimensions drift-diffusion theory becomes questionable. It remains valid, however, for base layers thicker than about 0.1 $\mu$m.[21]

Finally, the electron transit time across the collector space-charge layer is expressed by

$$\tau_{CT} = X_C/2v_d, \tag{11}$$

where $v_d$ is the mean free-electron drift velocity and the thickness of the collector space-charge layer is $X_c = X_4 - X_3$ (Fig. 1). As described in Sec. IV A, this thickness depends on the collector current.

Equation (11) requires that we specify the mean drift velocity in the base-collector space-charge layer. If that space-charge layer is reverse biased, the local electric field can change nearly abruptly with position near the base edge, causing velocity overshoot. For the reasons set forth in Sec. III, we neglect velocity overshoot and set the maximum ve-

locity equal to the scatter-limited or saturation velocity ($1.5\times10^7$ cm/s for GaAs at $T=300$ K).

From (1)–(11), we see that the cutoff frequency depends strongly on the base and collector layer thicknesses, $W_B$ and $X_c$, and their dependencies on the collector current and other variables.

### A. Base and collector thickness dependence on collector current

We focus on the base-collector homojunction space-charge layer. Since HBTs typically have low emitter and collector doping concentrations compared with the doping concentration of the base layer, we have $X_2 - X_{jE} \approx 0$ and $X_{jC} - X_3 \approx 0$. As indicated in Sec. III, the conventional silicon homojunction analysis of $W_B$ and $X_c$ to include high-collector-current effects remains valid. The physics underlying that analysis was described in Sec. II. We make the key simplifying step of dividing the idealized collector current density $J_c$ vs $V_{CE} = (V_{CB} + V_{BE})$ characteristics of an HBT into the six regions shown in Fig. 2. We assume forward-active operation.

In Fig. 2, $J_1$ and $J_2$ are given by[14,15]

$$J_1 = qN_{DC}v_s, \text{ and } J_2 = qN_{DC}\mu_n V_{CE}/W_C, \tag{12}$$

where $\mu_n$ is the electron mobility and $W_C = X_{jB} - X_{jC}$ is the metallurgical collector thickness (Fig. 1). The voltage $V_C$ (Fig. 2) at which $J_1 = J_2$ is given by[14]

$$V_C = W_C v_s/\mu_n. \tag{13}$$

#### 1. $J_C \ll J_1 \ll J_2$ (region I) and $J_C \ll J_2 \ll J_1$ (region II)

In these regions, the base-collector junction is reverse biased and the transistor is in the forward-active mode. No base pushout occurs because $J_C < J_1$ in region I and $J_C < J_2$ in region II.[14] Thus

$$W_B = X_{jC} - X_{jE}. \tag{14}$$

Next consider $X_C$. Let $X_0$ be the collector-base space-charge-layer thickness when $J_C = 0$.[22] If $V_{CE}$ is held constant and if $J_C$ is increased, two tendencies exist. One tendency, which dominates in region I, causes $X_C$ to expand (expansion mode) beyond $X_0$. The other tendency, which dominates in region II, causes $X_C$ to shrink (contraction mode) below $X_0$. The physics underlying the expansion and contraction modes was explained in Sec. II. To describe $X_C$, from Refs. 14 and 15, we have

$$X_C = X_0[(1 - J_C/J_2)/(1 - J_C/J_1)]^{0.5}, \tag{15}$$

for $X_C < W_C$. For $J_C$ approaching $J_1$ and for $V_{CE} \gg V_C$ in region I, the total collector layer becomes the space-charge layer ($X_C = W_C$); on the other hand, as $J_C$ approaches $J_2$ in region II, $X_C$ approaches zero.

#### 2. $J_1 \ll J_C \ll J_2$ (region III)

We define $J_{C\text{-}C}$ as an onset current given by[14]

$$J_{C\text{-}C} = qv_s(2\epsilon_C V_{CB}/qW_C^2 + N_{DC}). \tag{16}$$

For $J_C < J_{C\text{-}C}$, the collector layer is fully depleted in the expansion mode, but the quasineutral base has not thickened. Thus

$$W_B = X_{jC} - X_{jE}, \text{ and } X_C = W_C. \tag{17}$$

On the other hand, if $J_C \geq J_{C\text{-}C}$,[14] base pushout occurs and[23]

$$X_C = (X_{jB} - X_{jC})[(J_{C\text{-}C} - J_1)/(J_C - J_1)]^{0.5},$$

and

$$W_B = (X_{jC} - X_{jE}) + (X_{jB} - X_{jC} - X_C). \tag{18}$$

#### 3. $J_2 \ll J_C \ll J_1$ (region IV), $J_2 \ll J_1 \ll J_C$ (region V), and $J_1 \ll J_2 \ll J_C$ (region VI)

For these regions, the transistor operates in either the quasisaturation or the saturation mode. The base-collector junction voltage is $V'_{CB} = V_{CB} - V_D$. Here $V_D$ is the voltage drop in the undepleted collector layer. It is either a small forward voltage or a large forward voltage ($V'_{CB}$ is negative even though $V_{CB}$ is positive). Therefore, $X_C$ shrinks toward zero (contraction mode) and base pushout occurs. From the Kirk model,[15] we have

$$X_C \approx 0, \text{ and } W_B = (X_{jC} - X_{jE}) + W_C(1 - J_2/J_C). \tag{19}$$

More detailed yet less compact analytical models for $X_C$ and $W_B$ appear in Refs. 13 and 27. These relations suggest that the space-charge layer vanishes if $J_C < J_1$ (region IV), but it is induced in the collector layer if $J_C$ exceeds $J_1$ (regions V and VI).

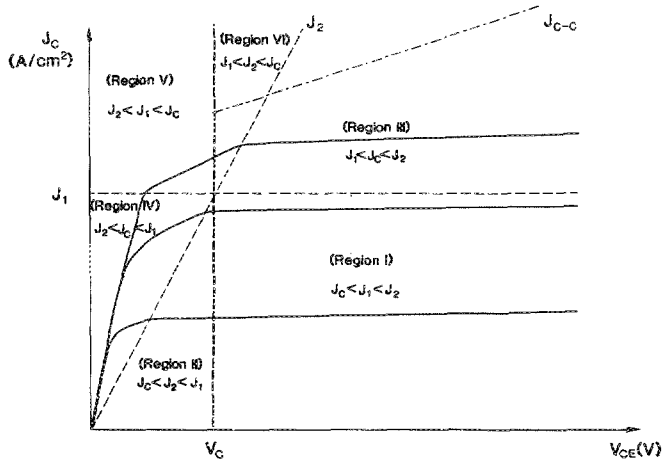


FIG. 2. Idealized collector current density $J_C$ collector-emitter applied voltage $V_{CE}$ characteristics dividing into six operation regions (regions I–VI). In the figure, $V_C$ is the voltage where $J_1 = J_2$.

TABLE I. Device makeup for the heterojunction bipolar transistor used in Figs. 3, 4, and 6.[a]

| Layer | Type | Doping ($10^{18}$ cm$^{-3}$) | Thickness ($\mu$m) |
|---|---|---|---|
| Cap | $n^+$-GaAs | 3.0 | 0.2 |
| Emitter | $n$-$Al_{0.3}Ga_{0.7}As$ | 0.5 | 0.1 |
| Base | $p^+$-GaAs | 10.0 | 0.1 |
| Collector | $n$-GaAs | 0.1 | 0.3 |
| Buffer | $n^+$-GaAs | 3.0 | 1.0 |
| Substrate | semi-insulating GaAs | Cr/$O_2$ | |

[a]Emitter-base junction area = 45 $\mu$m$^2$; base-collector junction area = 200 $\mu$m$^2$; for this device, $J_1 \approx 1.6\times10^5$ A/cm$^2$, $J_2 \approx 2\times10^6\times V_{CE}$ A/cm$^2$, and $V_C \approx 0.1$ V.

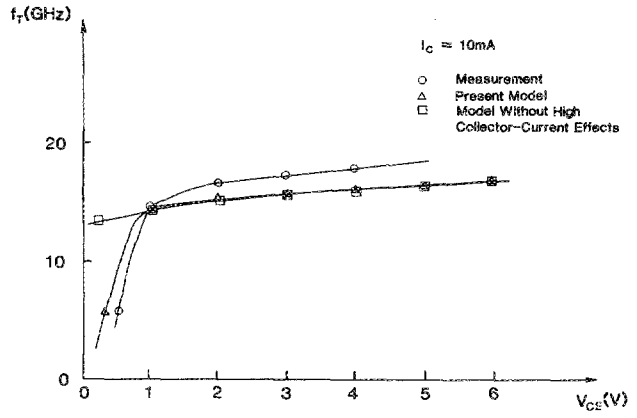


FIG. 3. Cutoff frequency $f_T$ vs $V_{CE}$ at $I_C = 10$ mA obtained from the present model, from a model without high-collector-current effects (Ref. 12), and from measurement (Ref. 6).

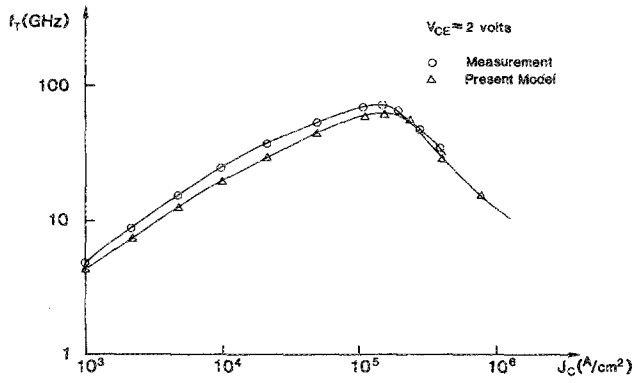


FIG. 5. Cutoff frequency $f_T$ vs $J_C$ at $V_{CE} = 2$ V calculated from the present model and from measurement (Ref. 28) for a slightly different device as that in Figs. 3 and 4.

## V. ILLUSTRATIONS AND CONCLUSIONS

For illustration, we use our model to calculate cutoff frequency for an MBE-grown AlGaAs/GaAs/GaAs high-performance heterojunction bipolar transistor,[6] which has become a standard in HBT technology, and we compare the results with experimental data in Ref. 6. The device makeup of the HBT is given in Table I. Figure 3 illustrates cutoff frequency versus $V_{CE}$, at collector current $I_C = 10$ mA, obtained in three ways: from measurement,[6] from our model, and from a cutoff frequency model without high-collector-current effects[12] that assumes $W_B = X_{jC} - X_{jE}$ and $X_C = X_0$.

The large discrepancies between the model without high-current effects and our model at low $V_{CE}$ result because the transistor operates in the saturation region (region IV or V). For such operation base pushout is significant and the base-collector space-charge-layer thickness deviates considerably from that at $I_C = 0$. Figure 4 plots cutoff frequency versus $I_C$ at $V_{CE} = 2$ V. It shows that our model predicts a falloff for $I_C > 100$ mA, which corresponds to $J_C > 2.2 \times 10^5$ A/cm$^2 > J_1$ (see Table I) and transistor operation in region III (see Fig. 2). In contrast, the model without high-collector-current effects increases monotonically as collector current increases.

Since measured cutoff frequency data for high currents are not available for this device, we compare our model with experimental data in Ref. 28 for a slightly different $Al_{0.3}Ga_{0.7}As$/GaAs/GaAs HBT, as shown in Fig. 5. This second transistor has the same device makeup as that in Table I except that the base doping concentration is $4 \times 10^{19}$ cm$^{-3}$, the collector doping concentration is $5 \times 10^{16}$ cm$^{-3}$, and the emitter junction depth is 0.15 $\mu$m. For all values of collector current, our model shows good agreement with measured results.

Figure 6 shows our model predictions for cutoff frequency versus collector-emitter voltage as a function of collector current for the same device used in Figs. 3 and 4. In this figure, cutoff frequency increases as collector current increases except for $I_C = 1000$ mA. At this high current, the cutoff frequency is smaller than that for $I_C = 100$ mA. It is apparent from Figs. 3–6 that HBTs possess high cutoff frequency and that cutoff frequency falloff will not occur until a very high-collector-current density is reached.

Our calculations show that cutoff frequency increases slightly with increasing $V_{CE}$ (Figs. 3 and 6), a trend that agrees with that predicted by Monte Carlo simulation re-

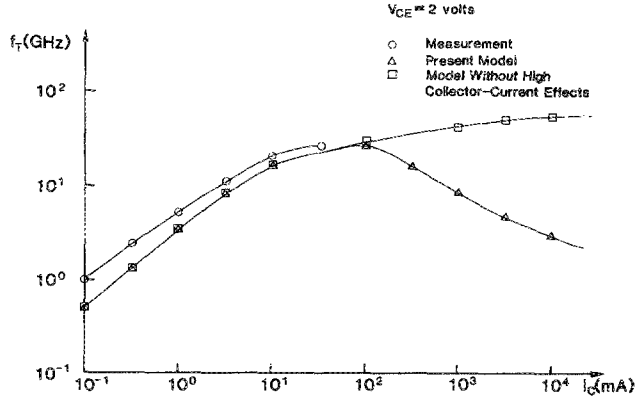


FIG. 4. Cutoff frequency $f_T$ vs $I_C$ at $V_{CE} = 2$ V obtained from the present model, from a model without high-collector-current effects (Ref. 12), and from measurement (Ref. 6).

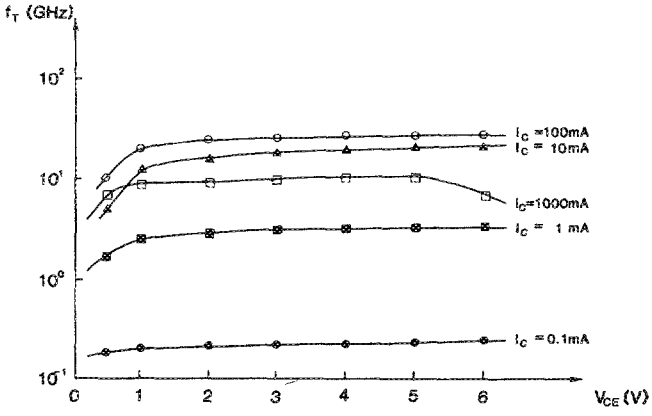


FIG. 6. Cutoff frequency $f_T$ vs $V_{CE}$ as a function of $I_C$ calculated from the present model.

ported by Rockett.[11] It contradicts, however, the experimental observations of Asbeck *et al.*,[9] Inada *et al.*,[29] and Yamuchi and Ishibashi,[30] all of whom measured a decrease in cutoff frequency with increasing $V_{CE}$. As explained by Rockett, the discrepancies occur because the collector capacitance in the measured devices was dominated by a parasitic component that was independent of the base-collector bias, a case that occurs in self-aligned HBTs with an ion-implanted extrinsic collector region. As a result, raising $V_{CE}$ in these devices will increase the collector transit time in the intrinsic transistor, but this increase will not be counterbalanced by a reduction of the collector charging time. In our model, only the intrinsic transistor is considered. In an intrinsic transistor, increasing $V_{CE}$ would increase the collector transit time. But simultaneously it would decrease the intrinsic base-collector junction capacitance by increasing the space-charge-layer thickness. This would decrease the collector charging time. Consequently, the net effects of $V_{CE}$ on cutoff frequency in forward-active mode are minimal in our model. More accurate modeling of the cutoff frequency requires inclusion of extrinsic elements. The agreement between our calculations, which neglect velocity, and Monte Carlo simulation,[11] which includes any velocity overshoot that occurs, suggests the validity of the conclusions reached in recent studies[10,11,21] that the influences of velocity overshoot on the total transit time and cutoff frequency of HBTs are marginal.

We have developed a simple, analytical model for the intrinsic part of single-heterojunction bipolar transistors that accounts for the influence of high collector current on cutoff frequency. The model has no fitting parameters. Comparison with experimental data for two transistors showed good agreement with model predictions. The model included base pushout and collector thickness modulation. As a key to the analysis, we divided the output current-voltage characteristics into six regions and set forth analytical expressions describing each region. The development of these expressions assumed that at high electric fields the electron drift velocity saturated and assumed also that conventional drift-diffusion analysis applied. For high-power applications, for which the collector-base applied voltage is high, transfer of electrons from the $\Gamma$ to the $L$ valleys will invalidate the assumption of a simple saturation velocity. For very small devices, the validity of a drift-diffusion description is threatened and velocity overshoot may affect the cutoff frequency. Thus, for such transistors, and for transistors for which parasitic elements dominate, the model presented here may not suffice. That it does suffice, however, for a range of present-day devices is demonstrated by agreement between our model predictions and experiments, on the one hand, and Monte Carlo simulations on the other. Our model thus adds the circuit and device design tools for heterojunction bipolar transistors.

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